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Signature

Applicant	:	Oscar E. Agazzi
Application No.	:	09/989,367
Filed	:	November 20, 2001
Title	:	METHOD AND SYSTEM TO IDENTIFY AND CHARACTERIZE NONLINEARITIES IN OPTICAL COMMUNICATIONS CHANNELS
Grp./Div.	:	2633
Examiner	:	Not yet assigned
Docket No.	:	41281/RJP/B600

INFORMATION DISCLOSURE STATEMENT
37 CFR § 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 7068
Pasadena, CA 91109-7068
September 4, 2003

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, and in accordance with the provisions in the Manual of Patent Examining Procedure §§ 609 and 707.05(b), enclosed is FORM PTO/SB/08A/B listing the references that are known to applicant. Copies of each of the listed references are enclosed. This filing is timely because it is made during one of the periods described in 37 CFR § 1.97(b).

It is respectfully requested that the listed references be considered in the examination of this application and identified on the list of references cited on the patent issuing for this application.

Applicant also requests that an initialed copy of FORM PTO/SB/08A/B be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

Stephen D. Burbach
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626/795-9900

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Enclosures: PTO/SB/08A/B, w/references
MEE PAS524433.1-*-09/4/03 8:49 AM

FORM PTO/SB/08A/B (10-01)
Substitute for PTO-1449A/B

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Attorney Docket Number	**41281/RJP/B600**
Application Number	09/989,367
Filing Date	November 20, 2001
Applicant(s)	Oscar E. Agazzi
Group Art Unit	2633
Examiner Name	Not yet assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		HUMBLET, PIERRE A., et al., On the Bit Error Rate of Lightwave Systems with Optical Amplifiers, IEEE Journal of Lightwave Technology, November 1991, pgs. 1576-1582, Vol. 9, No. 11
		BLACK, WILLIAM C., JR., et al., Time Interleaved Converter Arrays, IEEE Journal of Solid-State Circuits, December 1980, pgs. 1022-1029, Vol. SC-15, No. 6
		ELLERSICK, WILLIAM, et al., GAD: A 12-GS/s CMOS 4-bit A/D Converter for an Equalized Multi-Level Link, 1999 Symposium on VLSI Circuits Digest of Technical Papers, pgs. 49-52
		ELLERSICK, WILLIAM, et al., A Serial-Link Transceiver Based on 8GSample/s A/D and D/A Converters in 0.25μm CMOS, IEEE International Solid State Circuits Conference, 2001/Session 4/High Speed Digital Interfaces/4.1, 3 pgs.
		YANG, CHIH-KONG KEN, et al., A Serial-Link Transceiver Based on 8-GSamples/s A/D and D/A Converters in 0.25-μm CMOS, IEEE Journal of Solid-State Circuits, November 2001, pgs. 1684-1692, Vol. 36, No. 11
		DALLY; WILLIAM J., et al., Transmitter Equalization for 4Gb/s Signalling, Proceedings of Hot Interconnects IV, Palo Alto, 1996, 10 pgs.

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

FORM PTO/SB/08A/B (10-01) Substitute for PTO-1449A/B **INFORMATION DISCLOSURE** **STATEMENT BY APPLICANT** (use as many sheets as necessary)	**Attorney Docket Number**	**41281/RJP/B600**
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	Applicant(s)	Oscar E. Agazzi
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OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		JENQ, YIH-CHYUN, Digital Spectra of Nonuniformly Sampled Signals: A Robust Sampling Time Offset Estimation Algorithm for Ultra High-Speed Waveform Digitizers Using Interleaving, IEEE Transactions on Instrumentation and Measurement, February 1990, pgs. 71-75 Vol. 39, No. 1
		EKLUND, JAN-ERIK, et al., Digital Offset Compensation of Time-Interleaved ADC Using Random Chopper Sampling, IEEE International Symposium on Circuits and Systems, May 2000, pgs. 447-450, Geneva, Switzerland
		FU, DAIHONG, et al., A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters, IEEE Journal of Solid-State Circuits, December 1998, pgs. 1904-1911, Vol. 33, No. 12
		IZZARD, M.J., et al., Analog versus Digital Control o a Clock Synchronizer for 3Gb/s Data with 3.0V Differential ECL, 1994 Symposium on VLSI Circuits Digest of Technical Papers, pgs. 39-40
		JIN, HUAWEN, et al., A Digital-Background Calibration Technique for Minimizing Timing-Error Effects in Time-Interleaved ADC's, IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing, July 2000, pgs. 603-613, Vol. 47, No. 7
		CONROY, CORMAC S.G., et al., An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1-μm CMOS, IEEE Journal of Solid-State Circuits, April 1993, pgs. 447-454, Vol. 28, No. 4
		YANG, CHIH-KONG KEN, Design Techniques for High-Speed Chip-to-Chip Links, Integrated Circuits and Systems Laboratory, University of California at Los Angeles 31 pgs.

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